Fig. 1 (a)

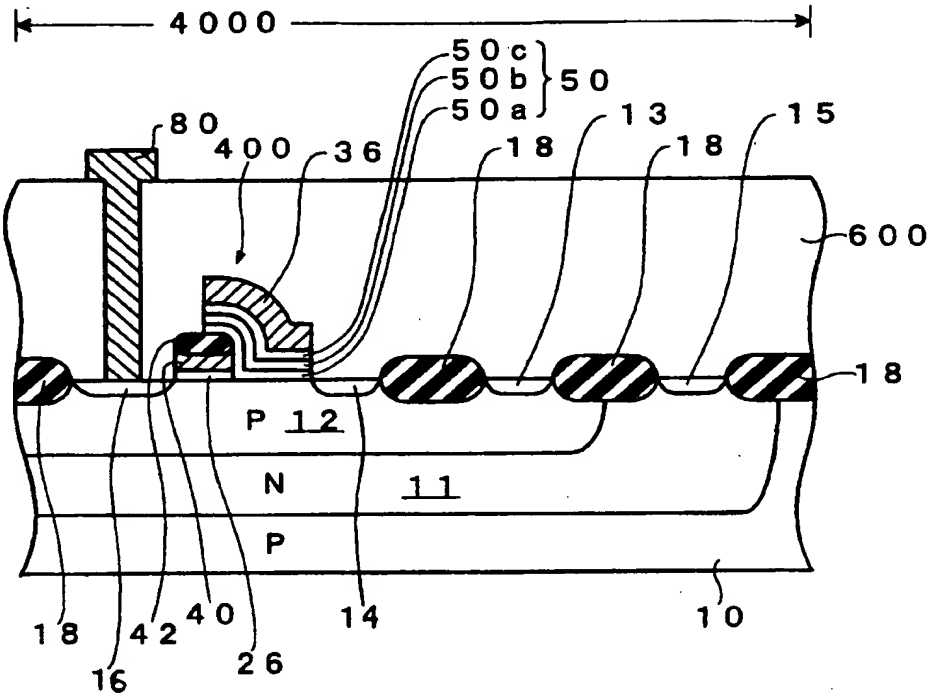

4000
50c
50b
50a
50
80
400
36
18
13
18
15
600
18
P 12
N 11
P
18
42
40
26
14
10
16

Fig. 1 (b)

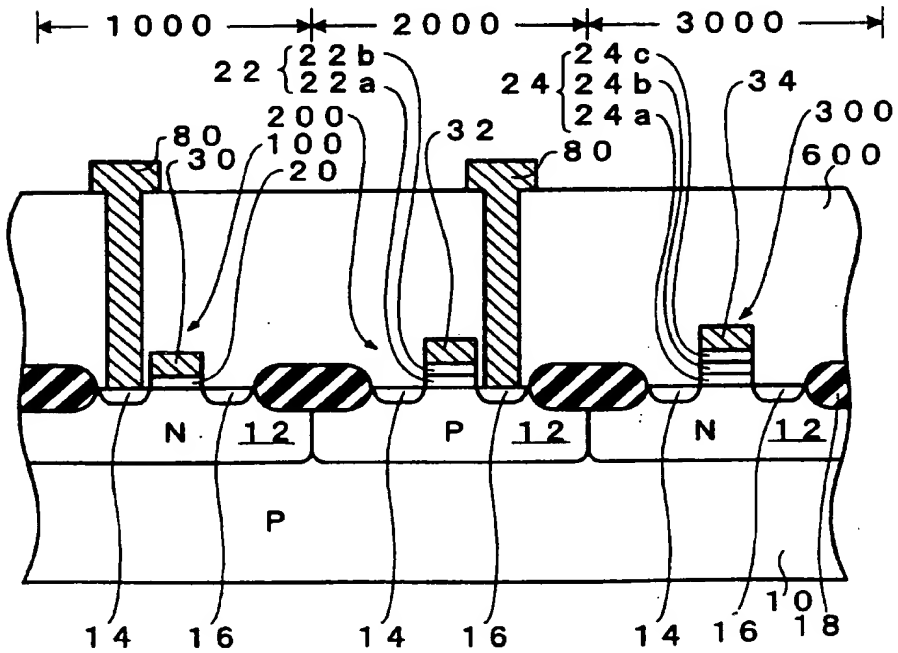

1000
2000
3000
22
22b
22a
24
24c
24b
24a
34
300
200
80
100
30
20
32
80
600
N 12
P 12
N 12
P
14
16
14
16
14
16
10
18

Fig. 2 (a)

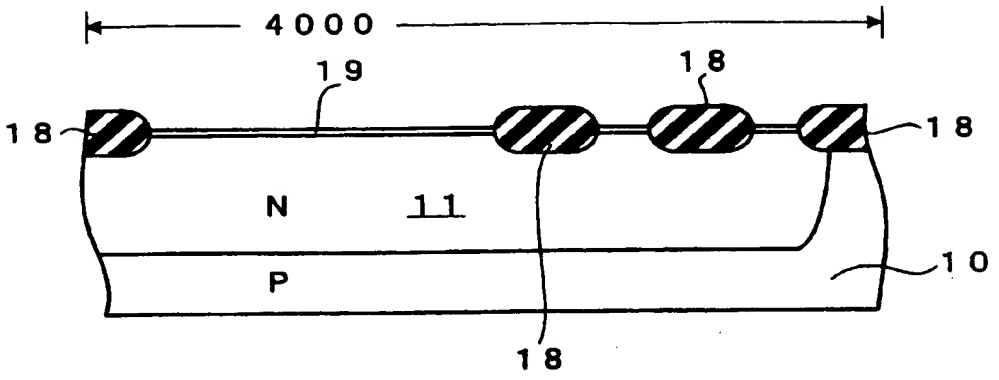
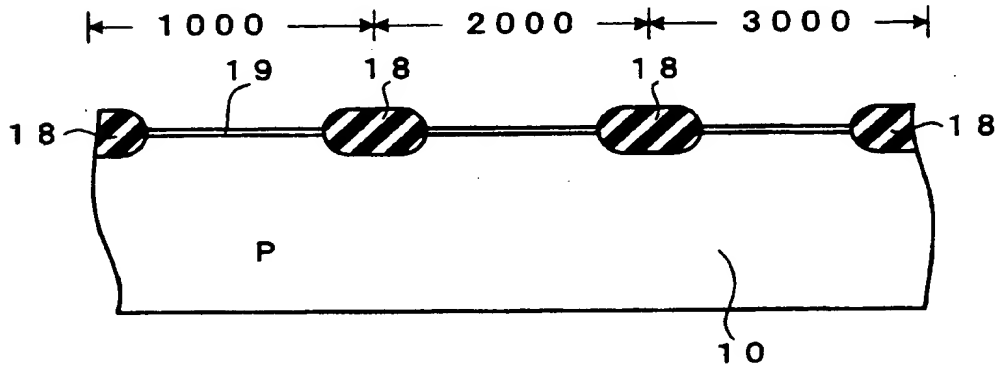


Fig. 2 (b)



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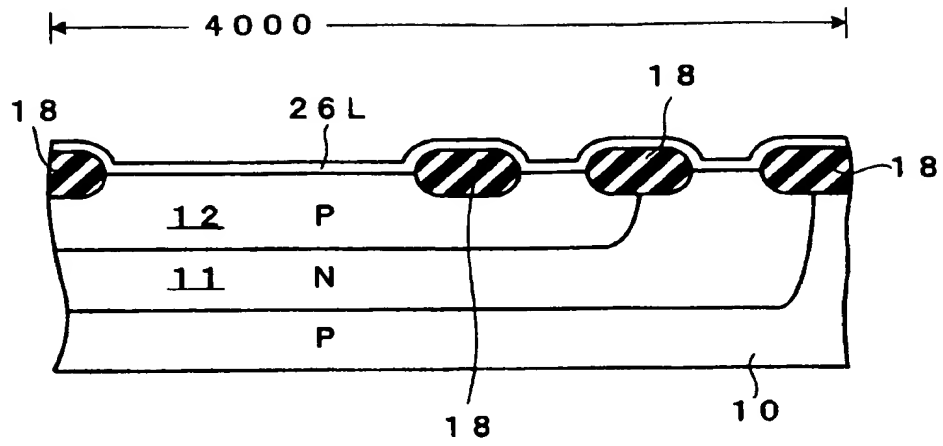

4000
18
18
26L
18
12
P
11
N
P
18
10

Fig. 3 (b)

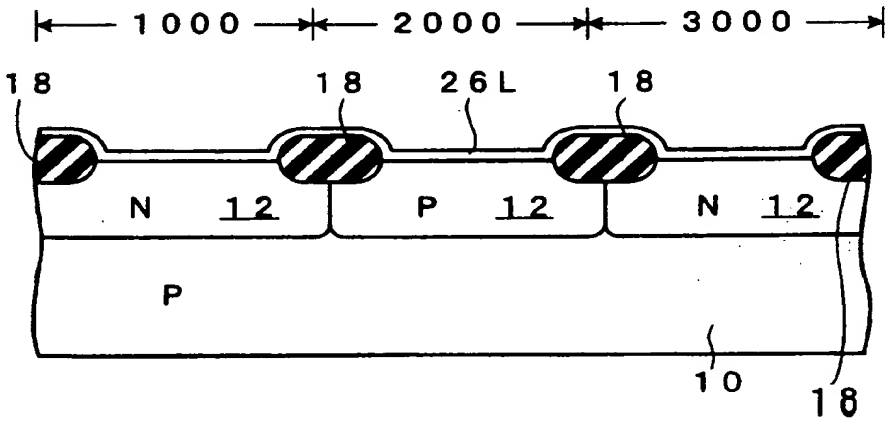

1000
2000
3000
18
18
26L
18
N
12
P
12
N
12
P
10
18

Fig. 4 (a)

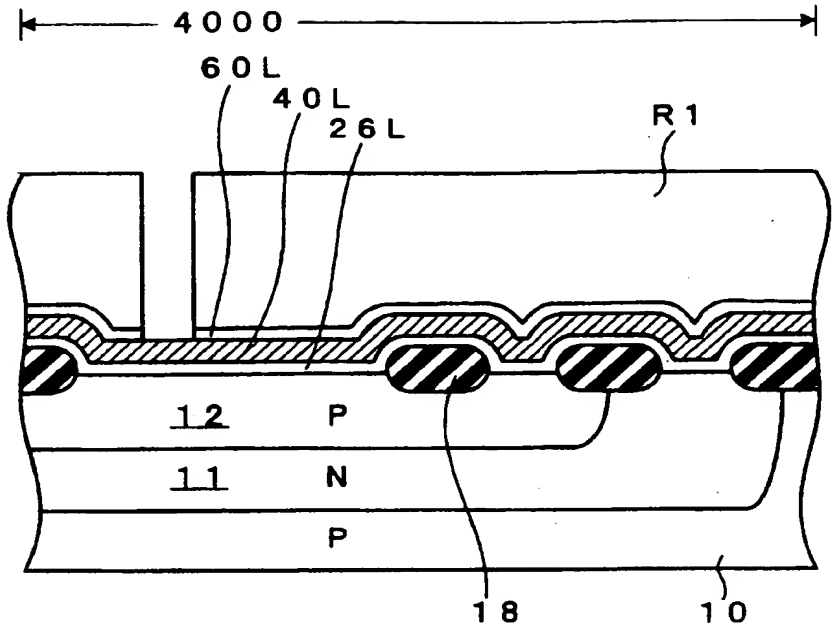

4000
60L
40L
26L
R1
12
P
11
N
P
18
10

Fig. 4 (b)

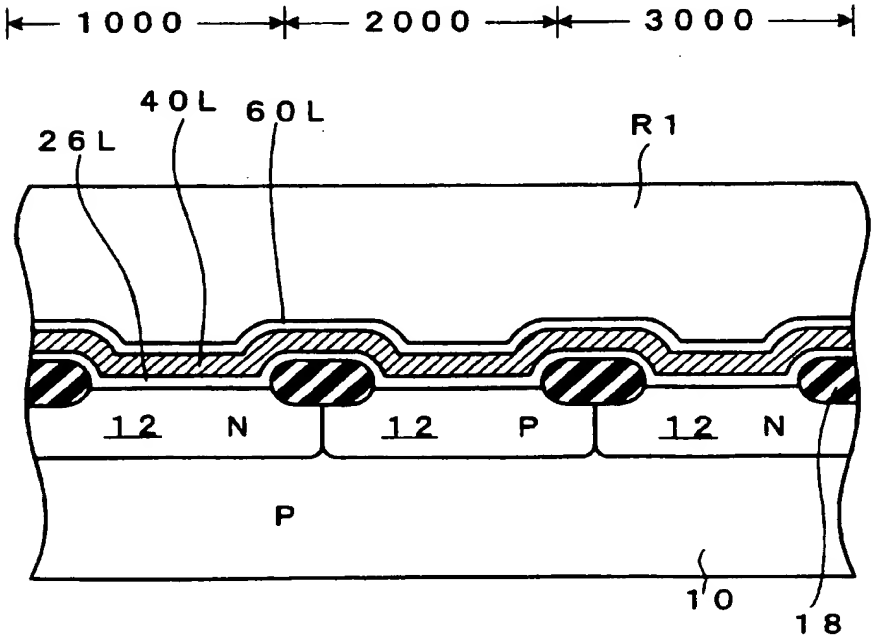

1000
2000
3000
40L
60L
26L
R1
12
N
12
P
12
N
P
10
18

Fig. 5 (a)

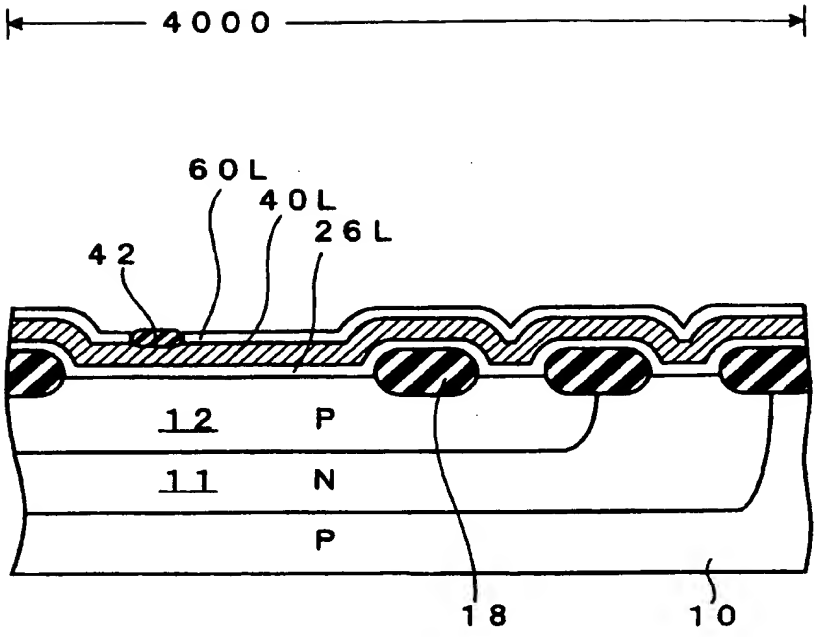

4000
60L
40L
26L
42
12
P
11
N
P
18
10

Fig. 5 (b)

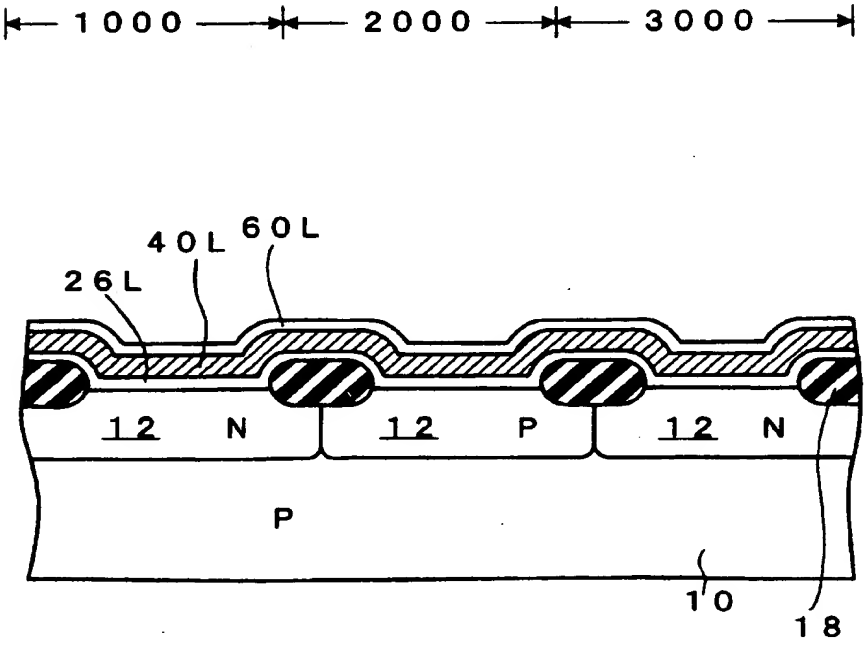

1000
2000
3000
40L
60L
26L
12
N
12
P
12
N
P
10
18

Fig. 6 (a)

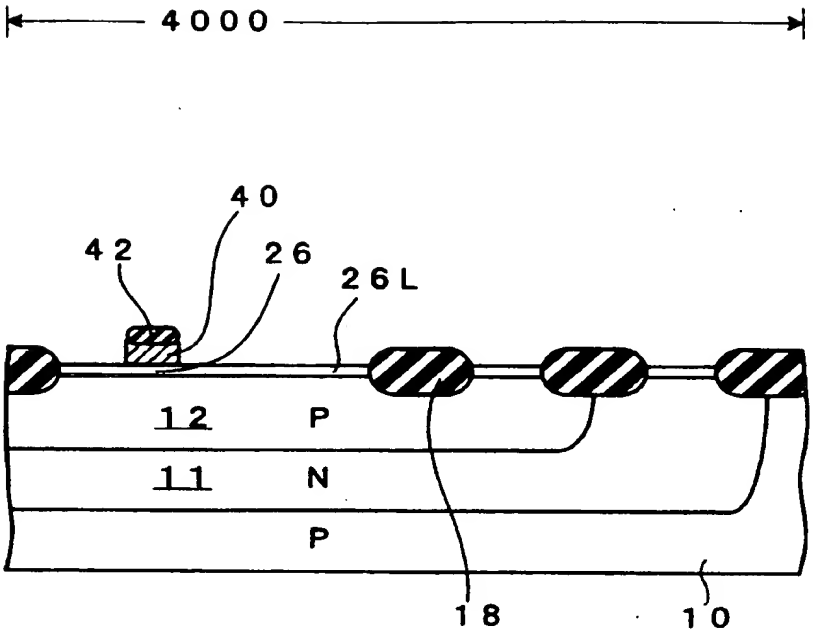

4000
40
42
26
26L
12
P
11
N
P
18
10

Fig. 6 (b)

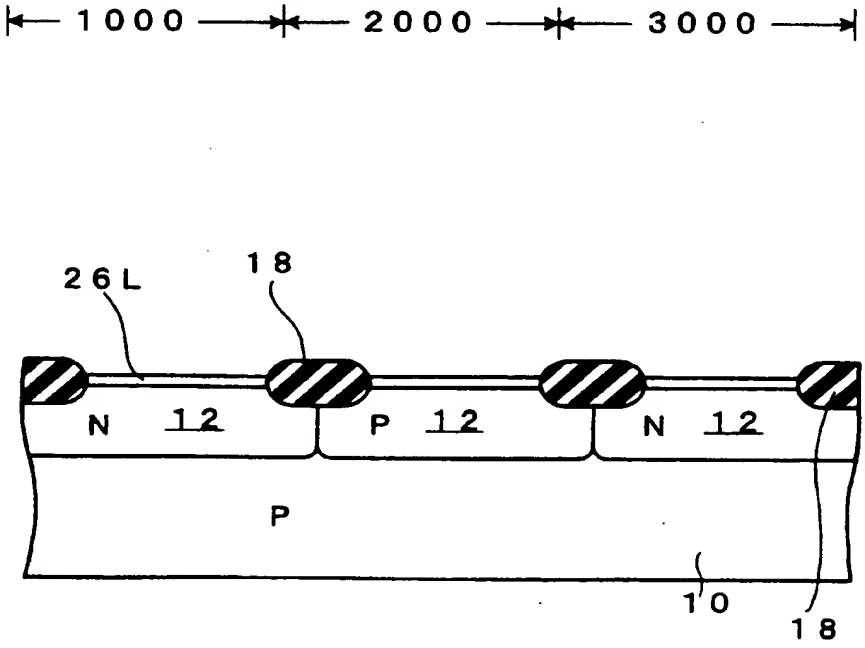

1000
2000
3000
26L
18
N
12
P
12
N
12
P
10
18

Fig. 7 (a)

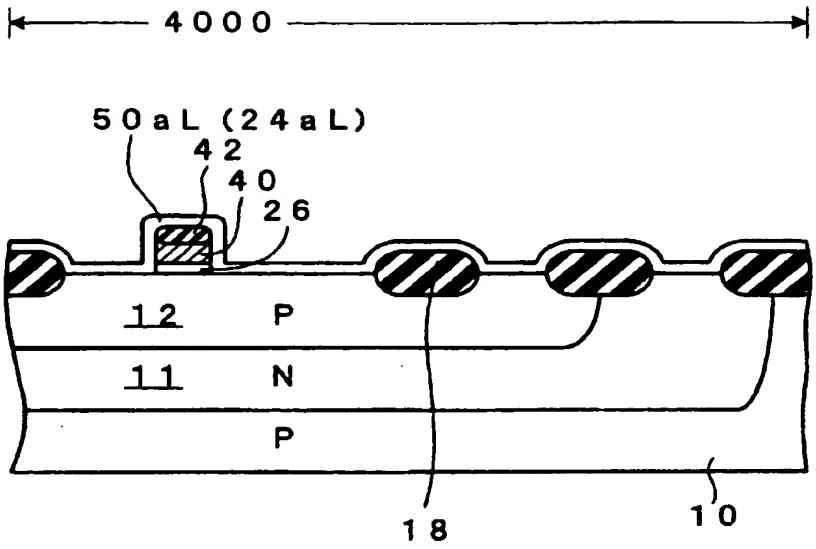

4000
50aL (24aL)
42
40
26
12
P
11
N
P
18
10

Fig. 7 (b)

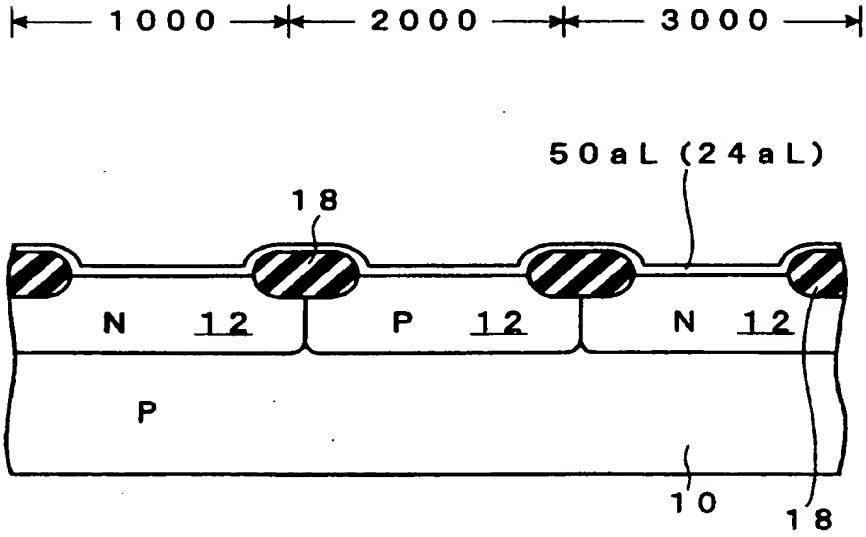

1000
2000
3000
50aL (24aL)
18
N
12
P
12
N
12
P
10
18

Fig. 8 (a)

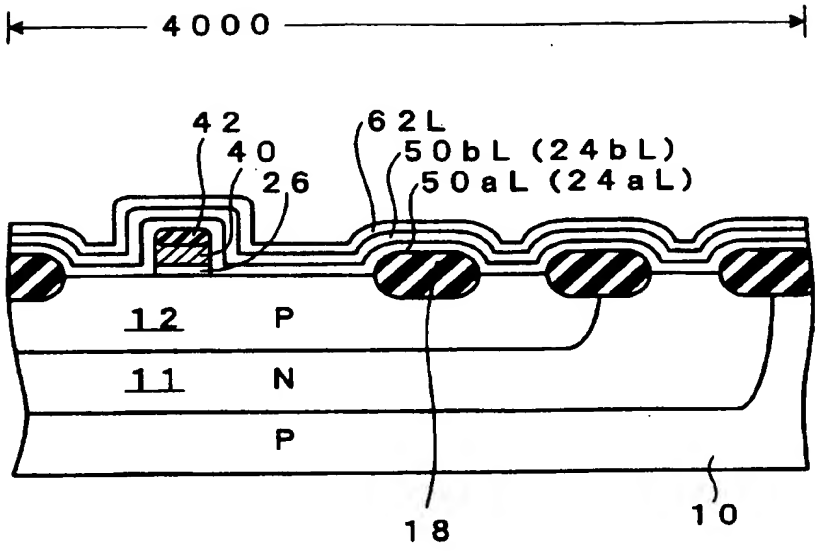

4000
42
40
26
62L
50bL (24bL)
50aL (24aL)
12
P
11
N
P
18
10

Fig. 8 (b)

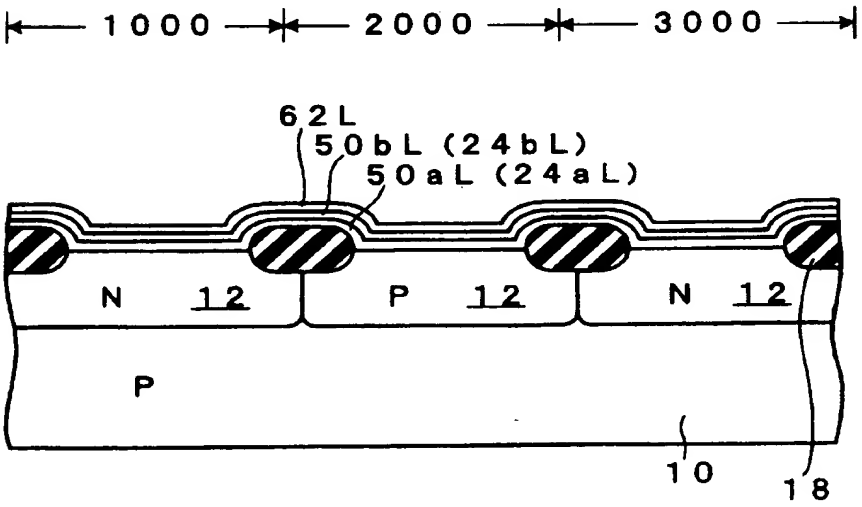

1000
2000
3000
62L
50bL (24bL)
50aL (24aL)
N
12
P
12
N
12
P
10
18

Fig. 9 (a)

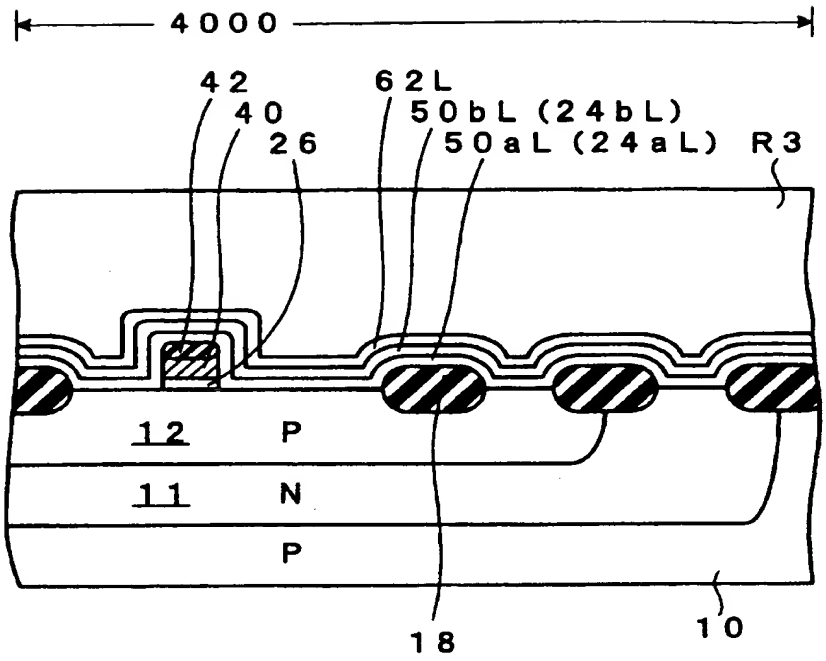

4000
42
40
26
62L
50bL (24bL)
50aL (24aL)
R3
12
P
11
N
P
18
10

Fig. 9 (b)

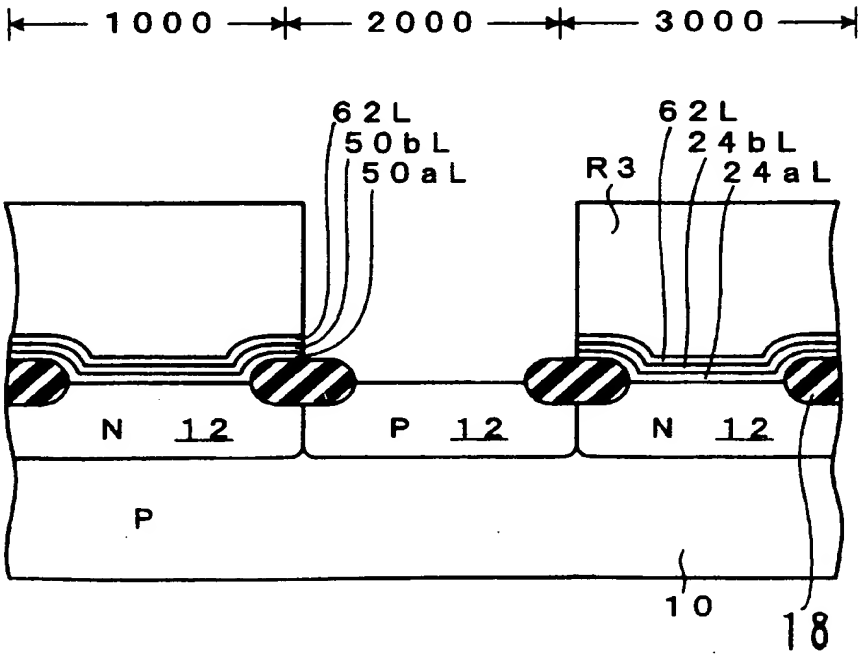

1000
2000
3000
62L
50bL
50aL
62L
24bL
24aL
R3
N 12
P 12
N 12
P
10
18

Fig. 10 (a)

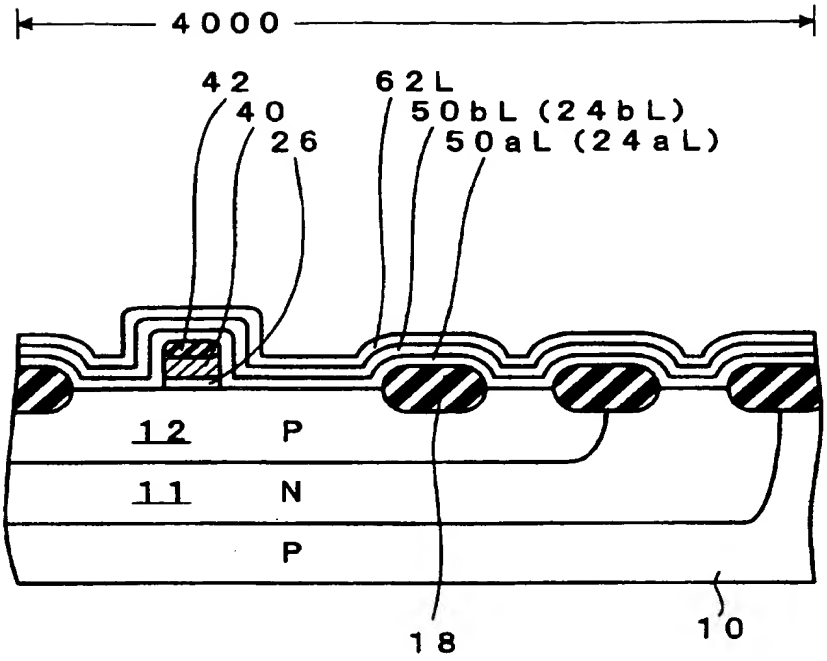
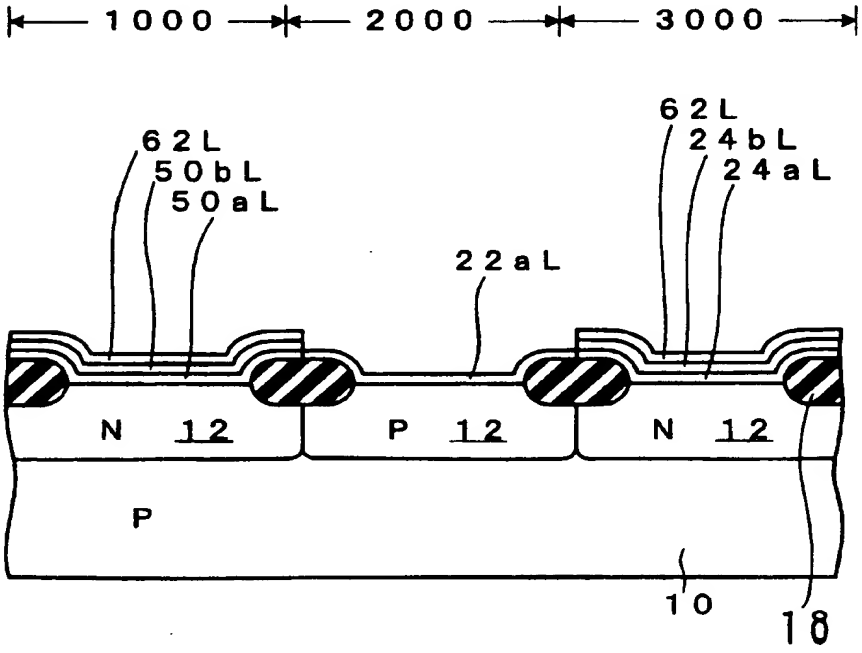


Fig. 10 (b)



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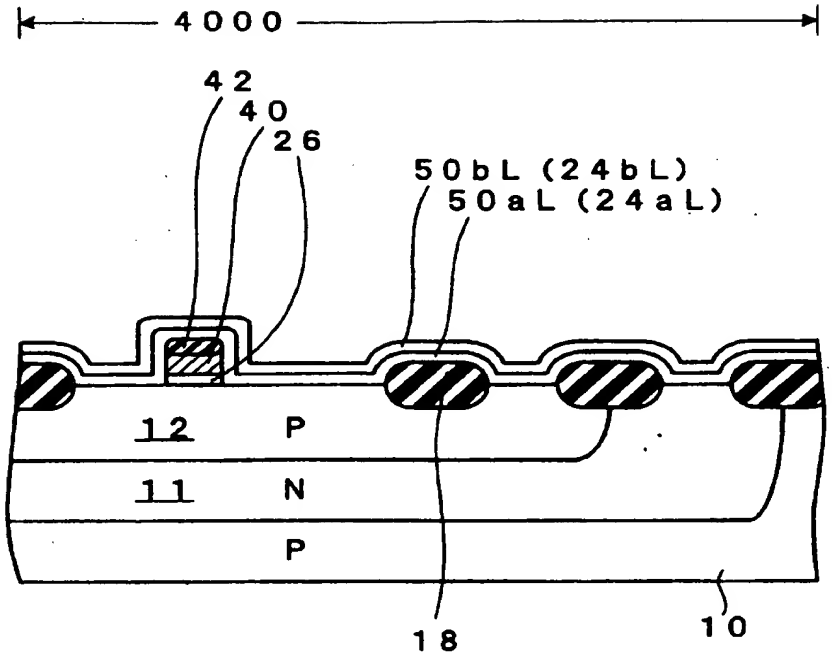


Fig. 11 (b)

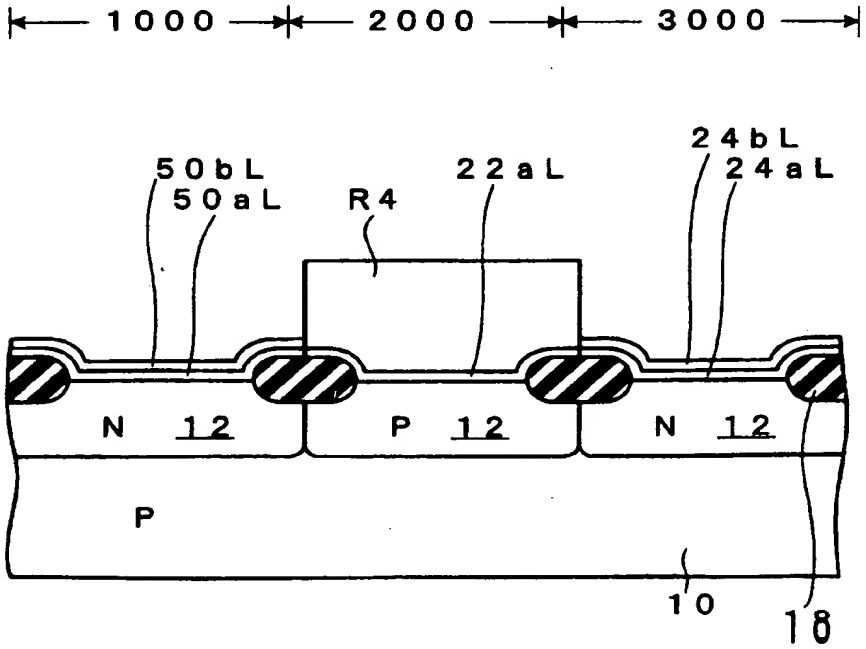


Fig. 12 (a)

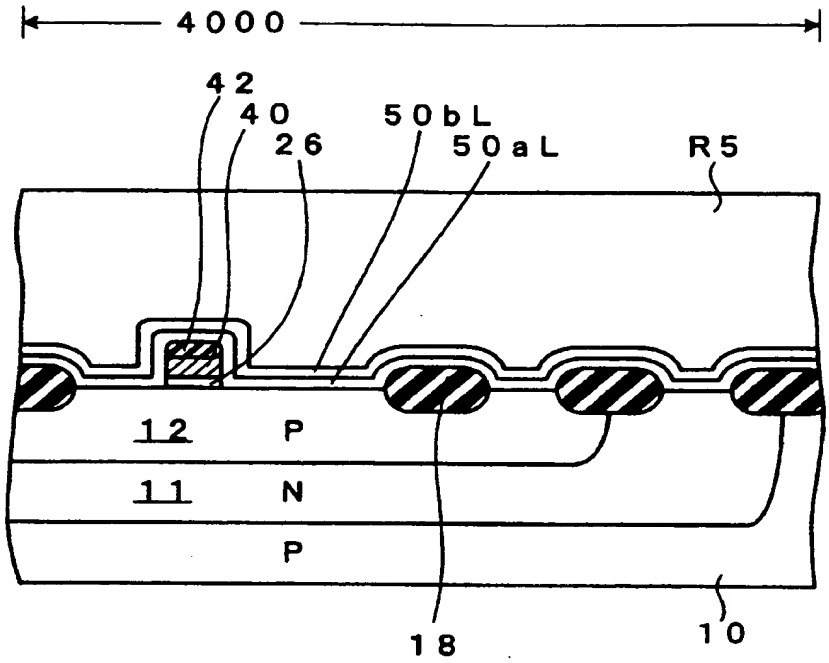


Fig. 12 (b)

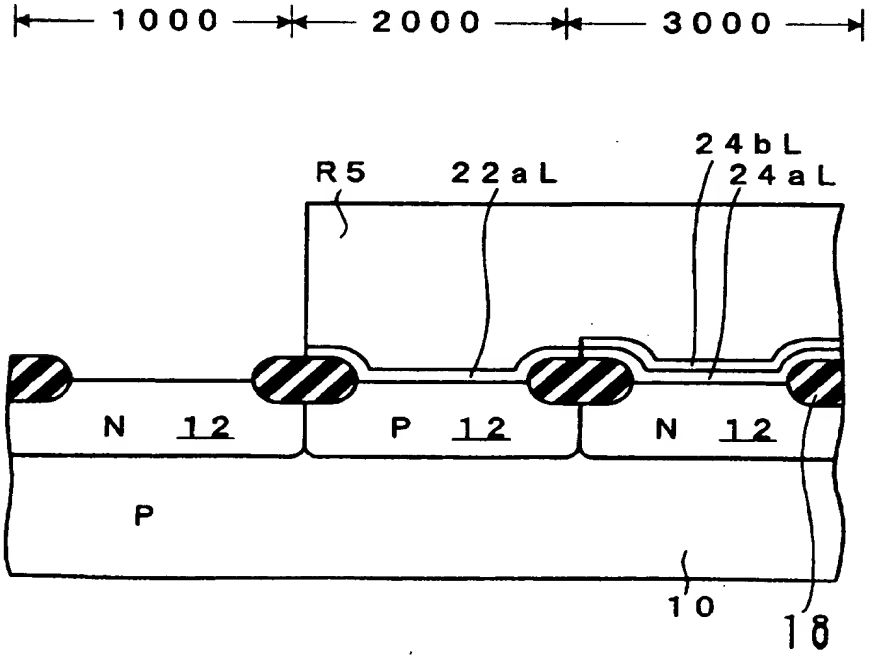


Fig. 13 (a)

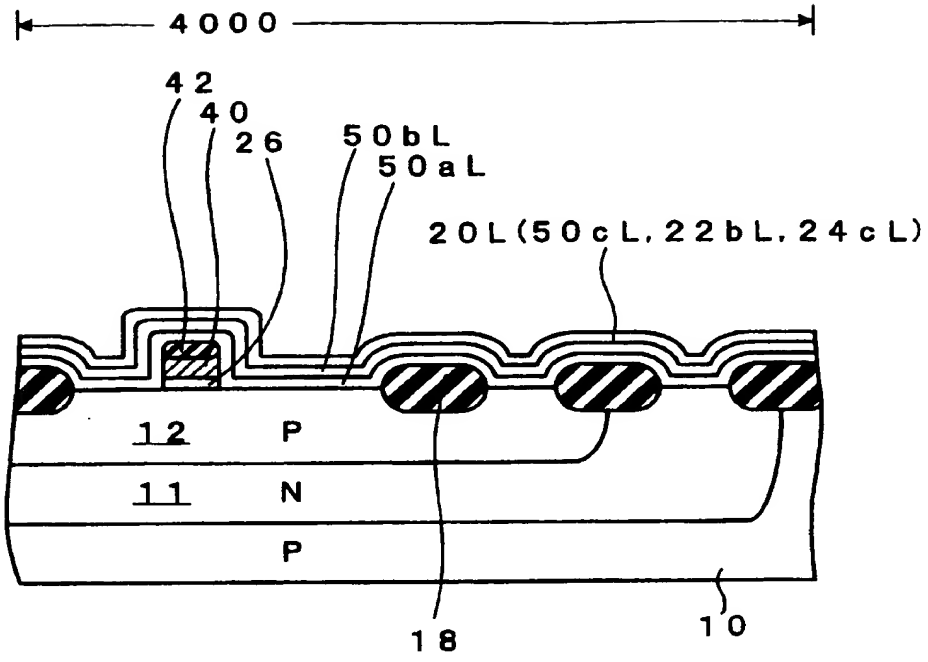
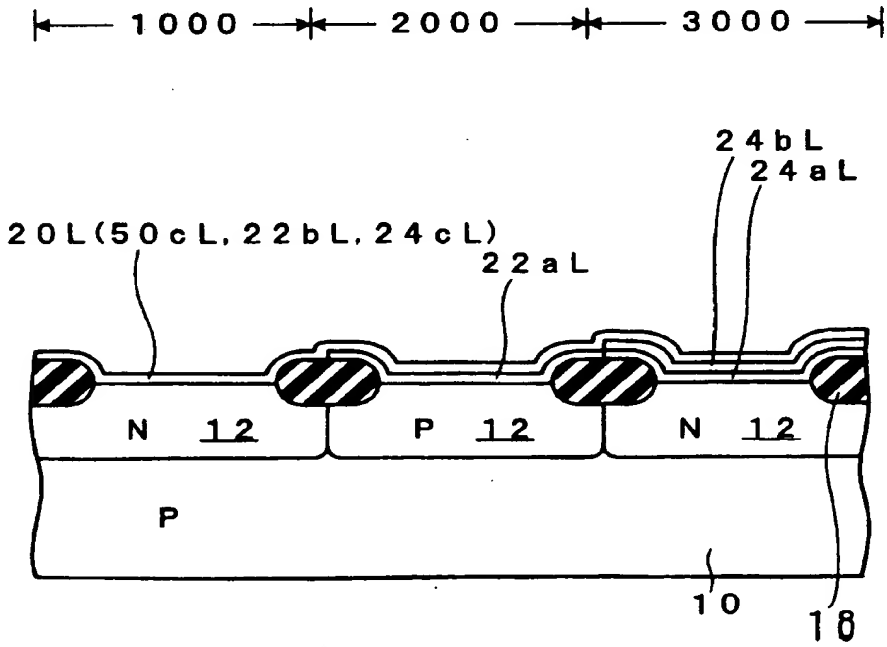


Fig. 13 (b)



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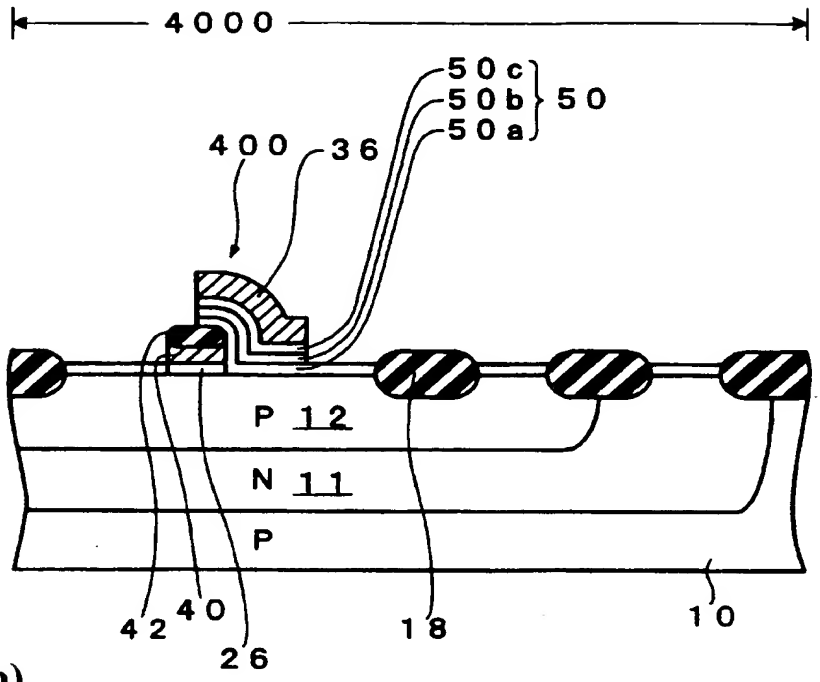
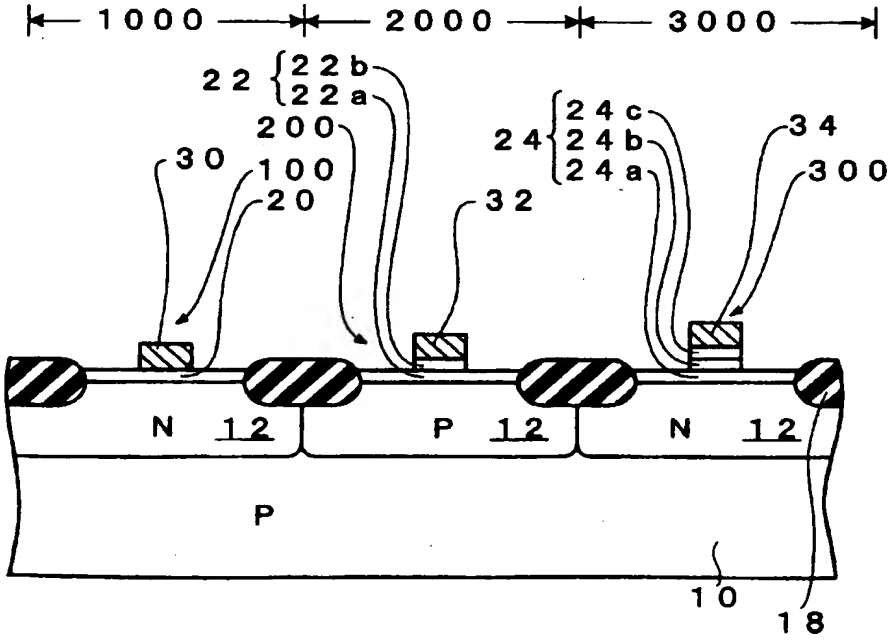


Fig. 14 (b)



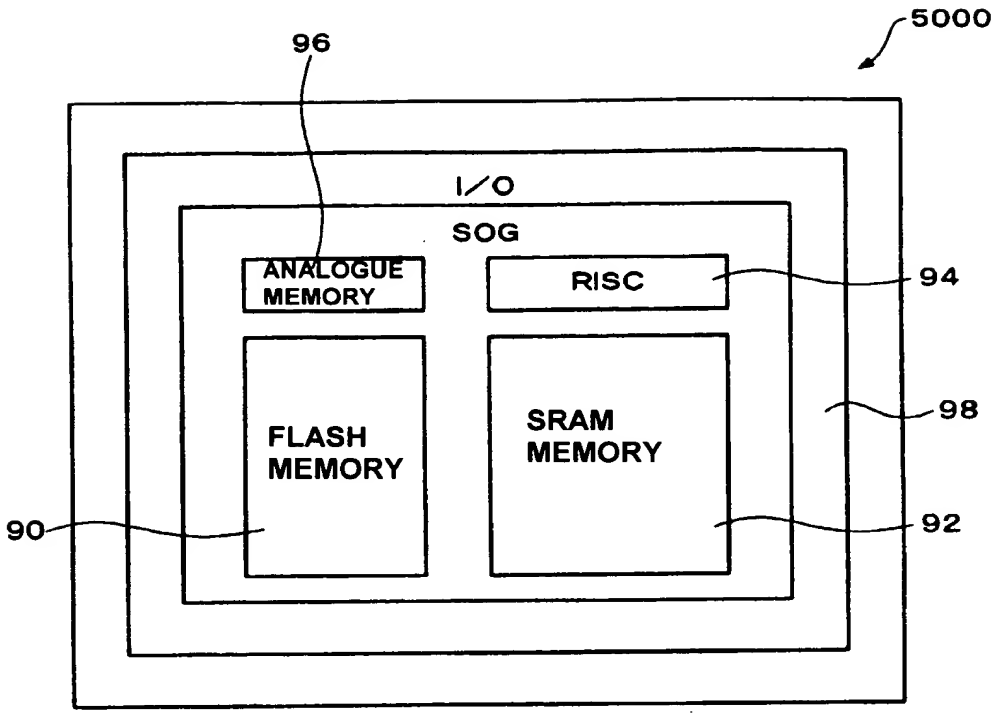

5000
96
I/O
SOG
ANALOGUE MEMORY
RISC
94
FLASH MEMORY
SRAM MEMORY
98
90
92

Fig. 15

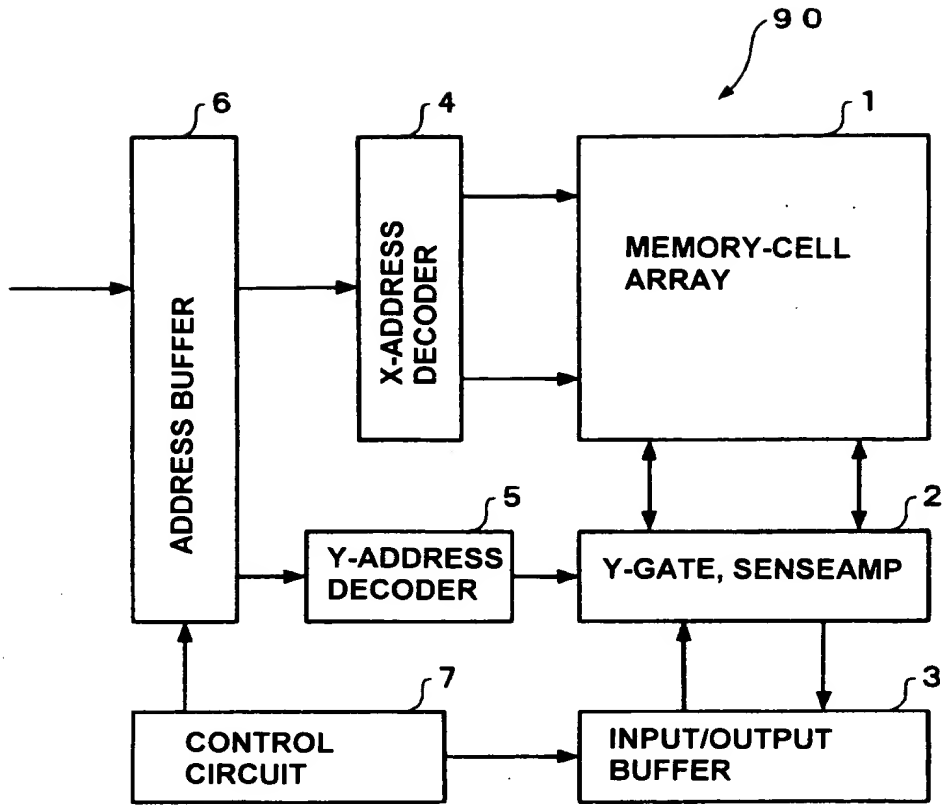

90
6
4
1
ADDRESS BUFFER
X-ADDRESS DECODER
MEMORY-CELL ARRAY
5
2
Y-ADDRESS DECODER
Y-GATE, SENSEAMP
7
3
CONTROL CIRCUIT
INPUT/OUTPUT BUFFER

Fig. 16